

FIG. 1(A) (PRIOR ART)

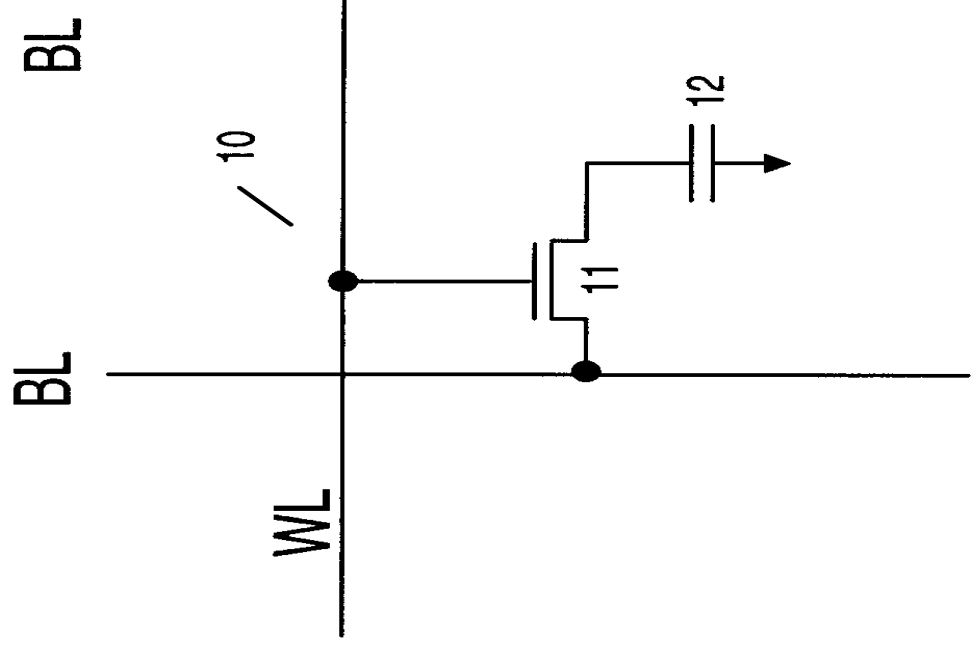
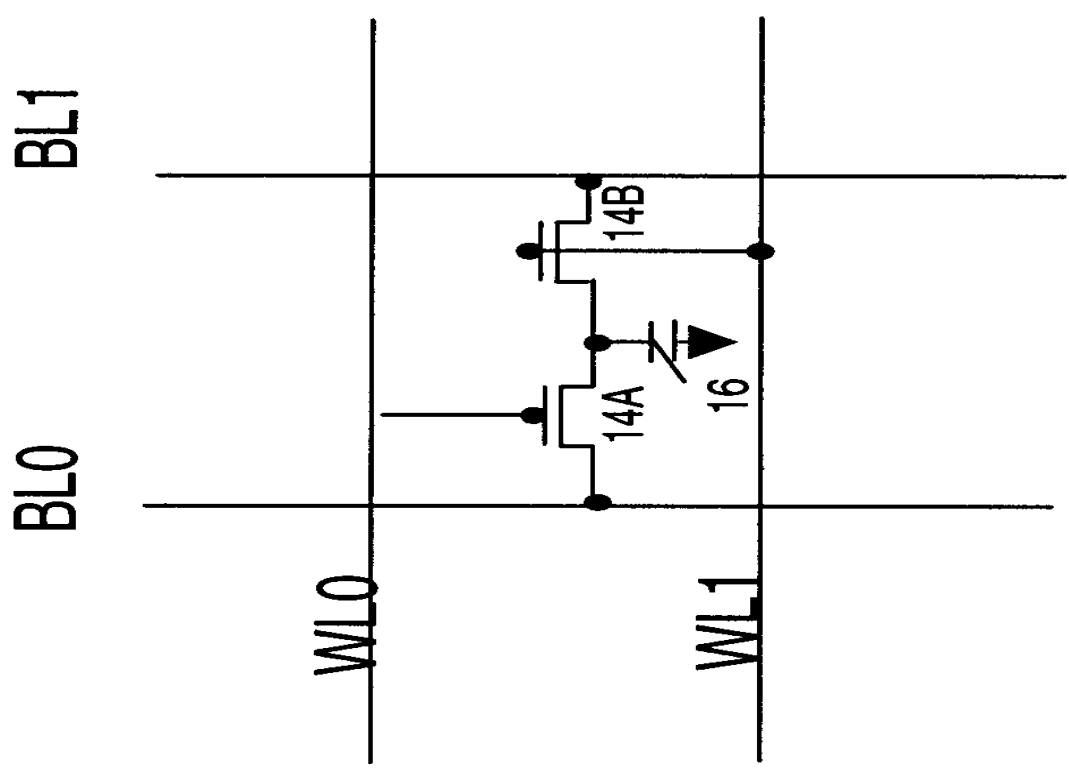
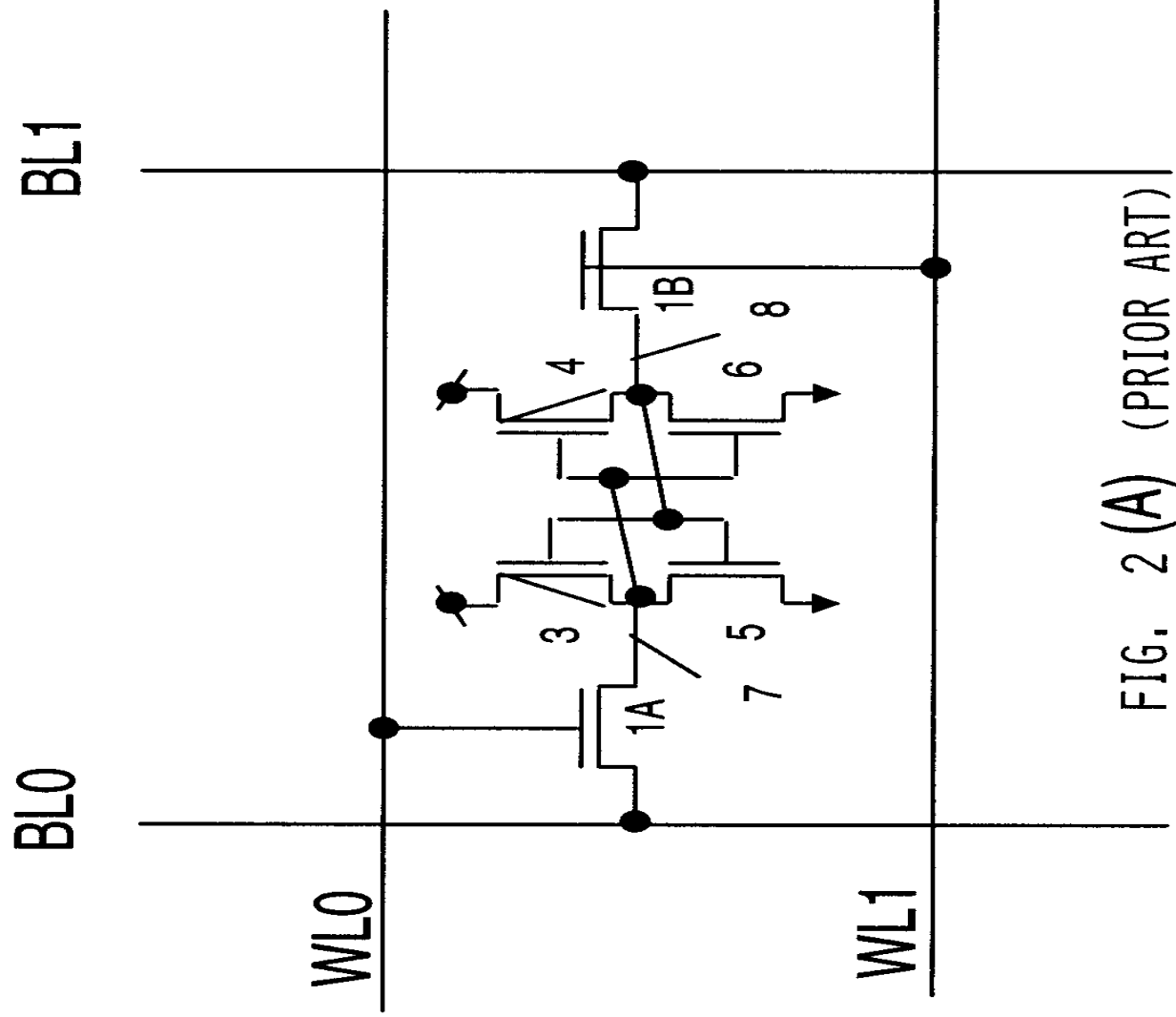


FIG. 1(B) (PRIOR ART)



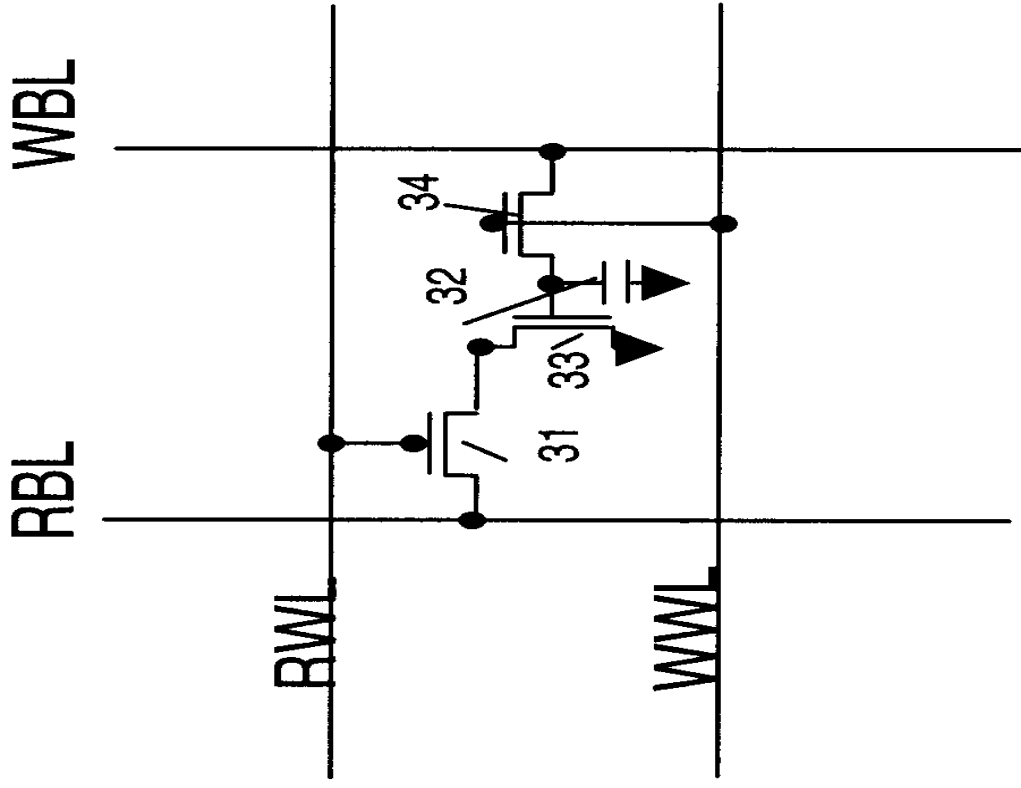


FIG. 3(A) (PRIOR ART)

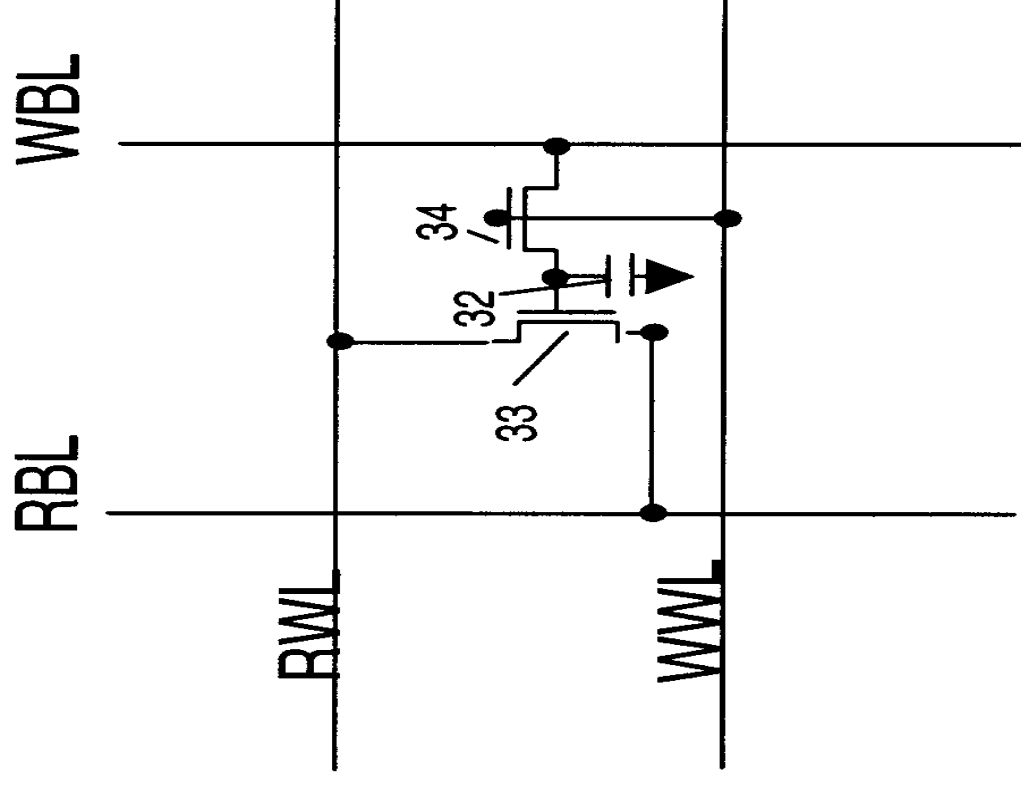


FIG. 3(B) (PRIOR ART)

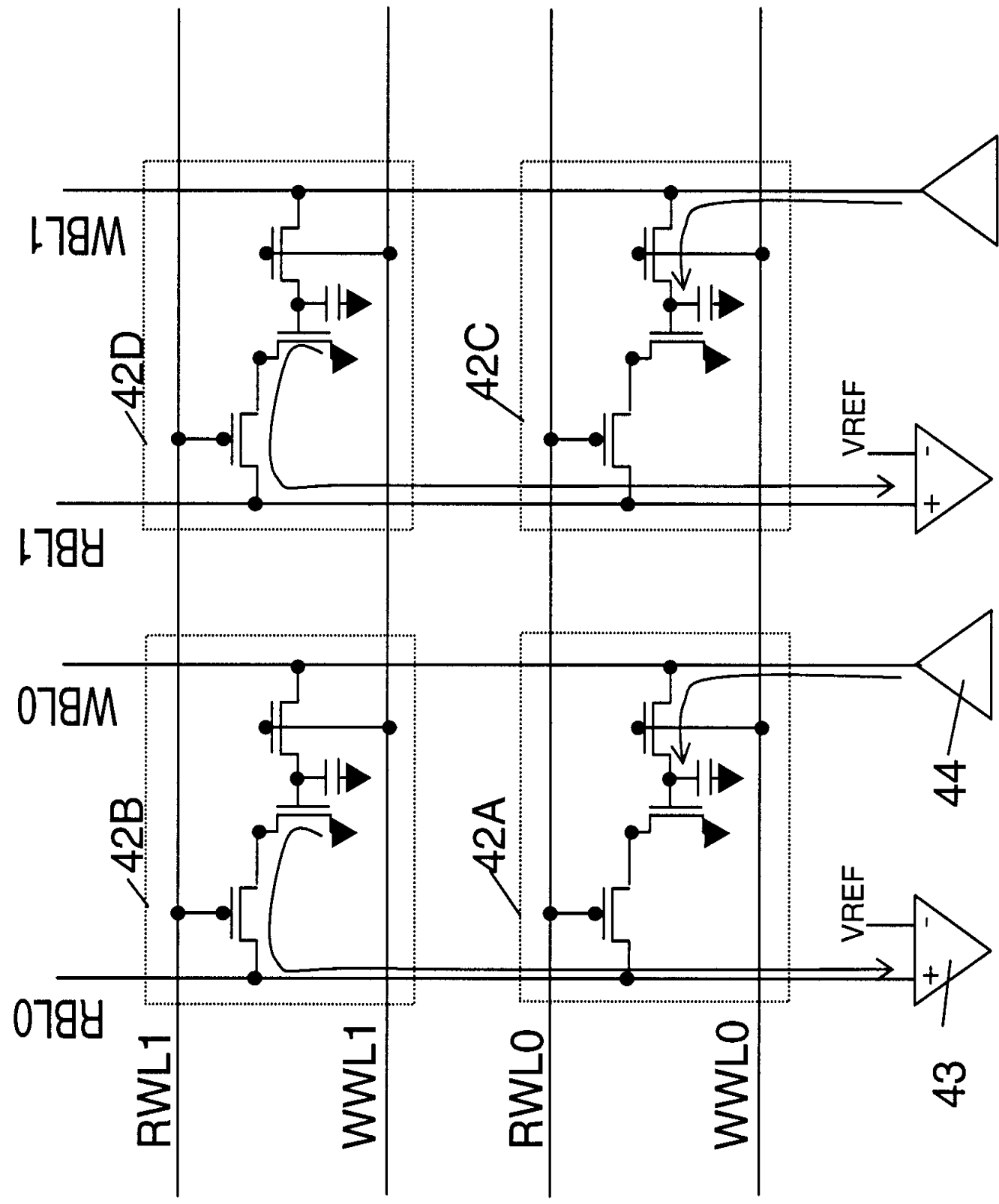


Fig. 4 (PRIOR ART)

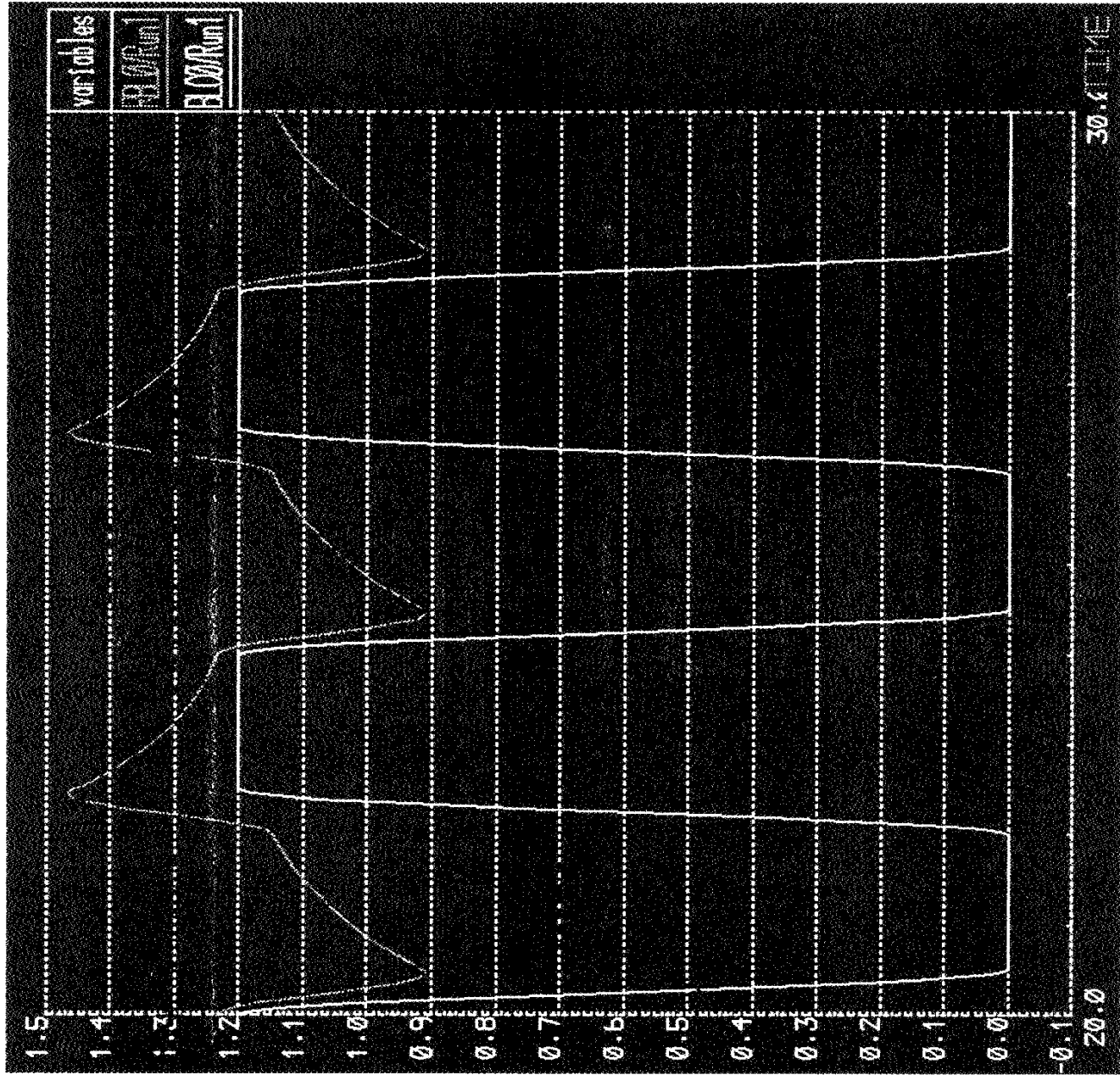
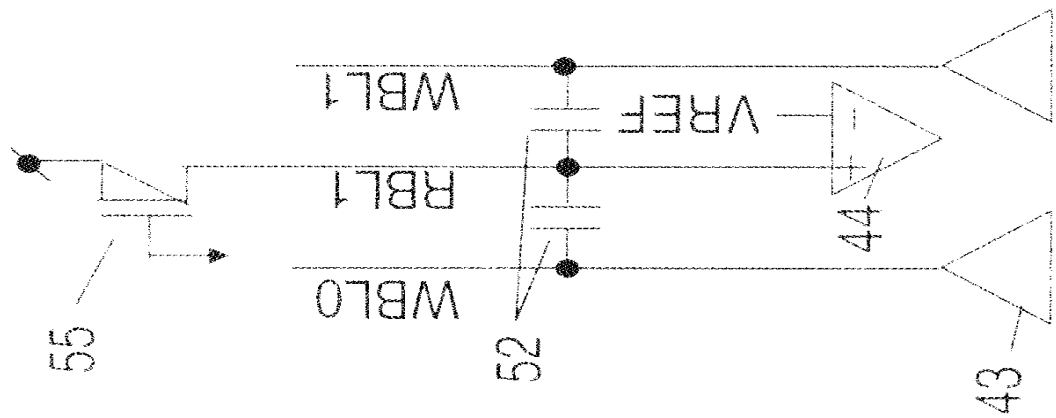


Fig. 5 (PRIOR ART)



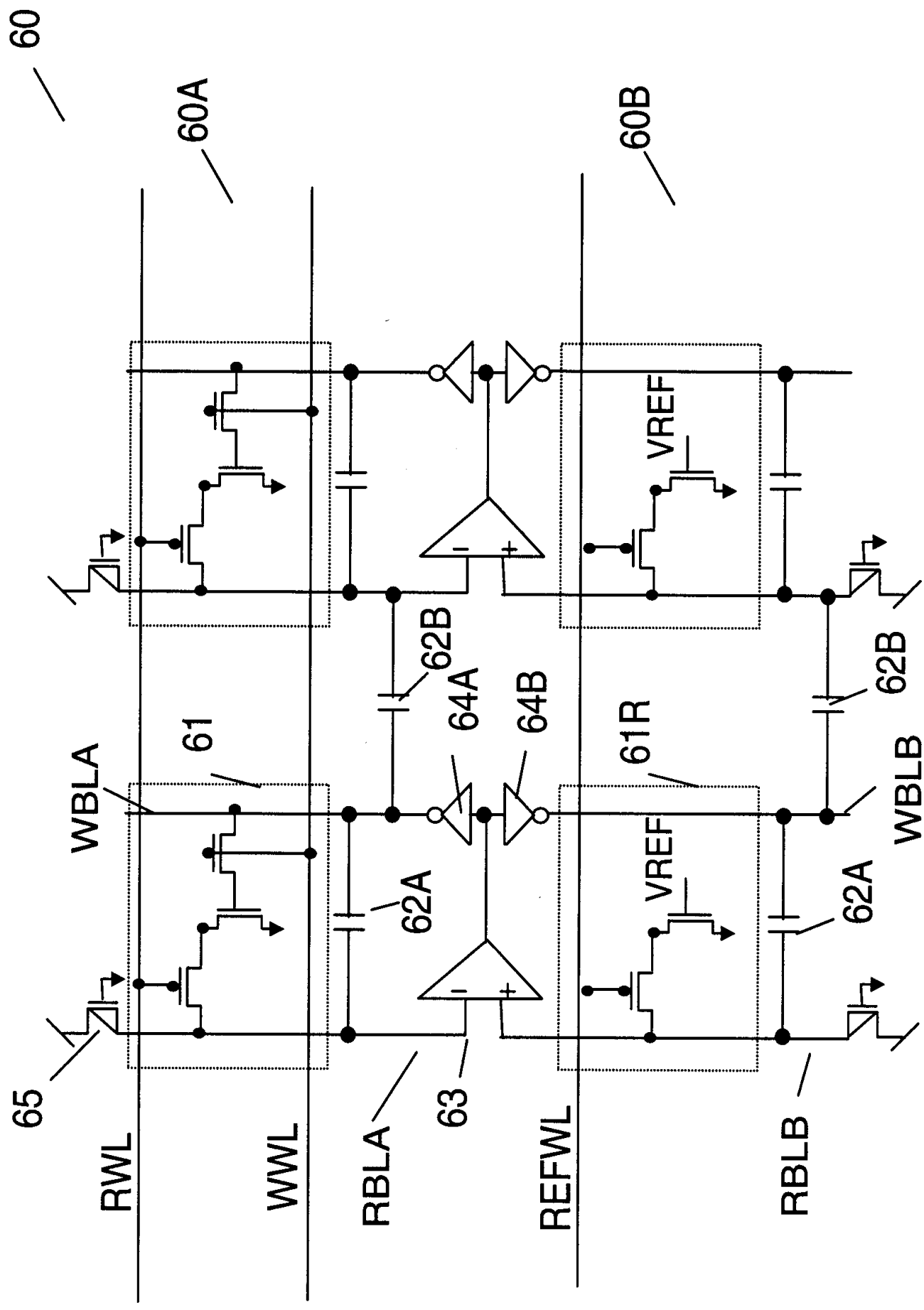
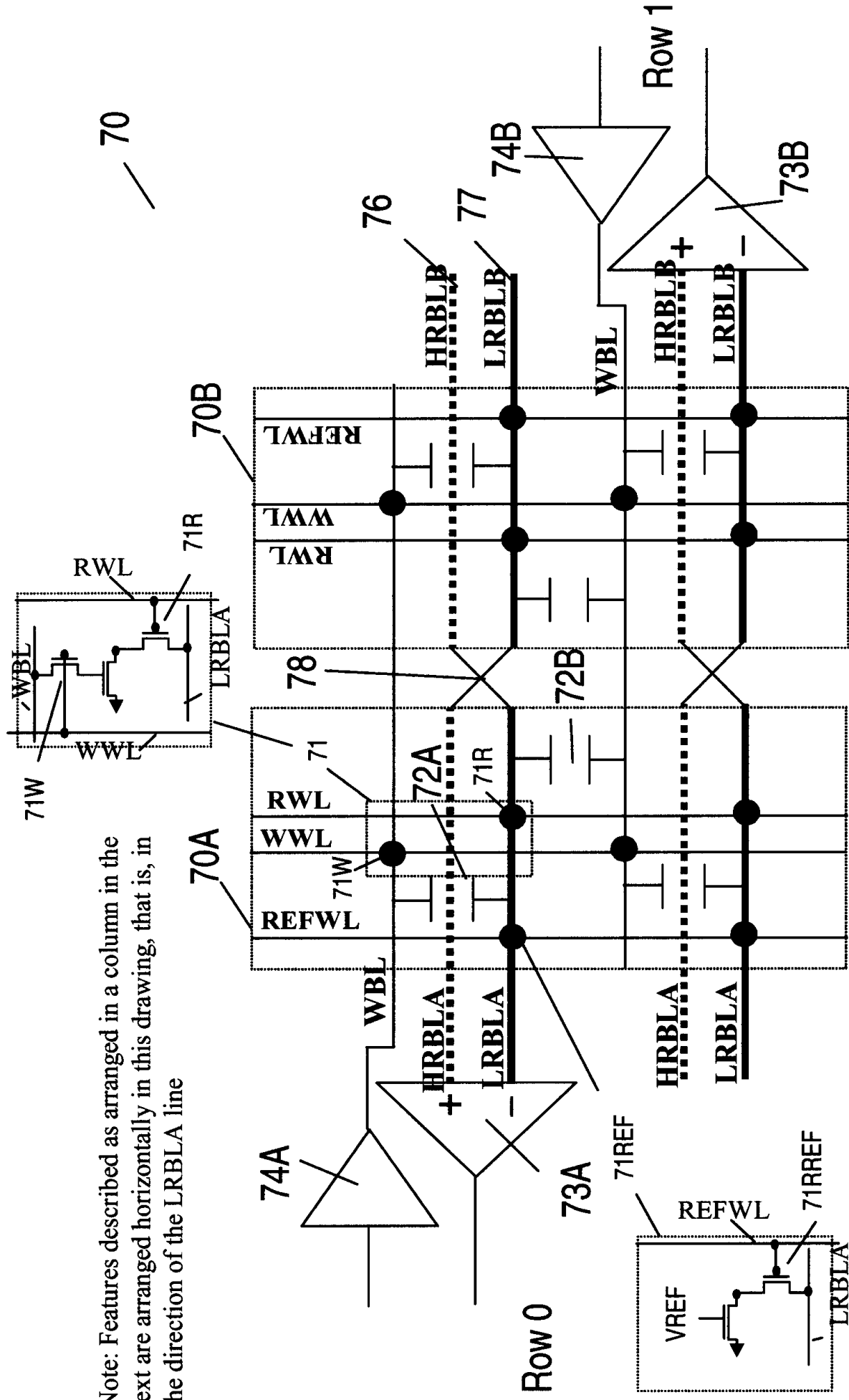


Fig. 6



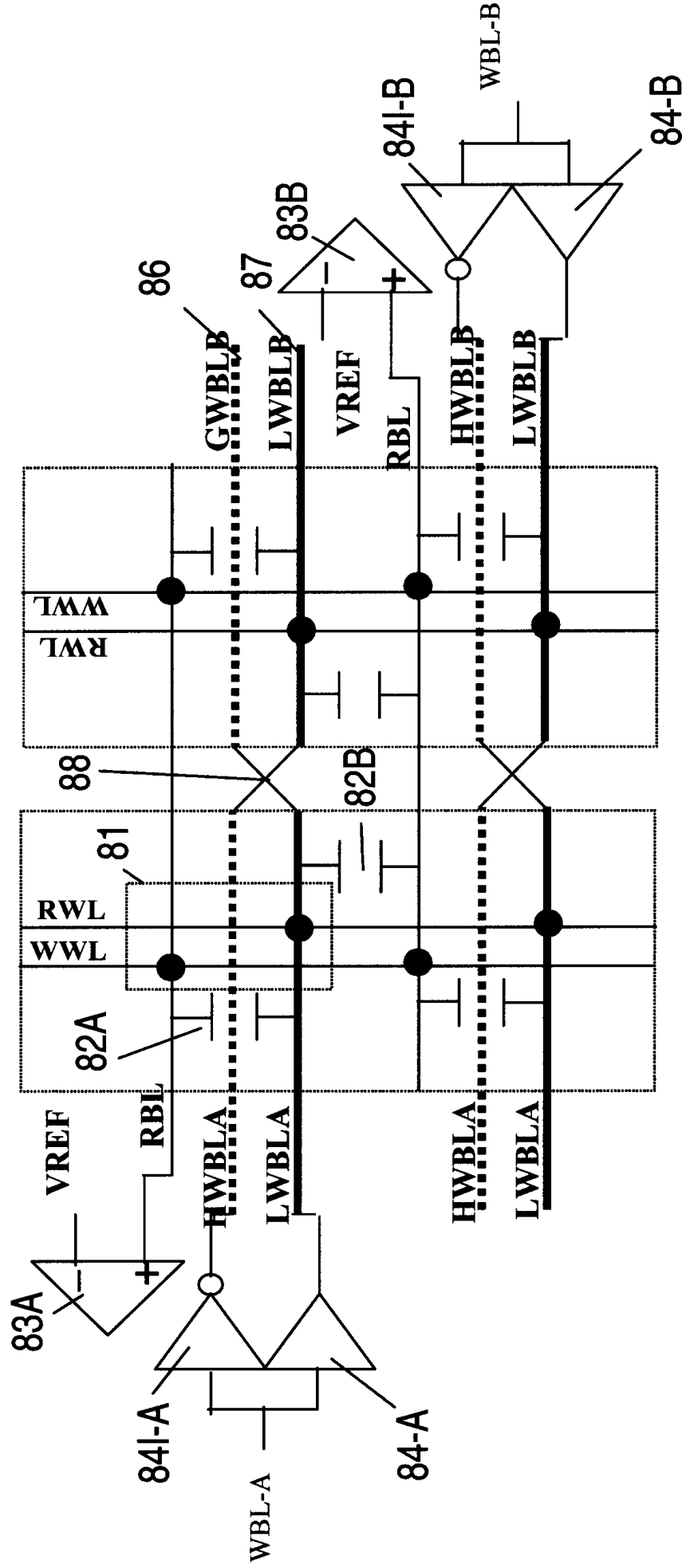
Note: Features described as arranged in a column in the text are arranged horizontally in this drawing, that is, in the direction of the LRBLA line

- Layer 1 —
- Layer 2 ·····
- Filled circle indicates a connection to a memory cell port

Fig. 7

Note: Features described as arranged in a column in the text are arranged horizontally in this drawing, that is, in the direction of the LRBLA line

80A 80B 80



Layer 1

Layer 2

Wires indicated by dotted lines are located on a different wiring layer than wires indicated by solid lines

Fig. 8